architecture rtl of regbank is

signal regs : array(0 to sz-1) of work.reg;

signal temp\_RD1, temp\_RD2 : bit\_vector(wd-1 downto 0);

begin

process(CLK)

begin

if rising\_edge(CLK) then

temp\_RD1 <= (others => '0');

temp\_RD2 <= (others => '0');

for r in 0 to sz-1 loop

if A1 = to\_unsigned(r, A1'length) then

temp\_RD1 <= regs(r).q;

end if;

if A2 = to\_unsigned(r, A2'length) then

temp\_RD2 <= regs(r).q;

end if;

if A3 = to\_unsigned(r, A3'length) and WE3 = '1' then

regs(r).en <= '1';

regs(r).d <= WD3;

else

regs(r).en <= '0';

end if;

end loop;

end if;

end process;

RD1 <= temp\_RD1;

RD2 <= temp\_RD2;

end rtl;